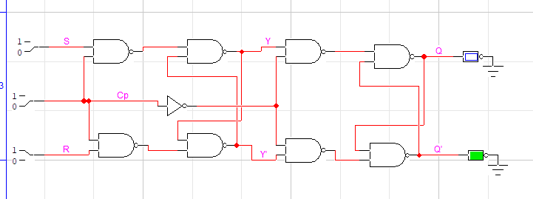
**Digital Logic Design (Lab – 11)**

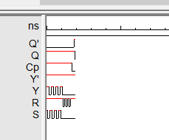
**Task 1:**

**Implement the SR Master-Slave flip flop on logic works. Also, show the timing diagram.**

**Logic Works Implementation:**

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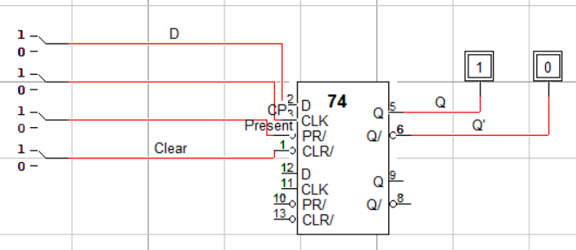
**Timing diagram:**

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**Task 2:**

Perform on Logic Works and test the ICs of D-Flip flop & JK flip flop so that is fulfils their tables (get familiar with inputs & outputs)

**D-Flip Flop IC 74\_74 test:**

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**Timing diagram:**

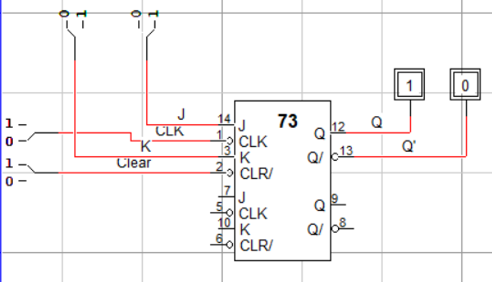


When CLR and pr are 1, value of output changes only due to edge triggering (positive) I.e.,

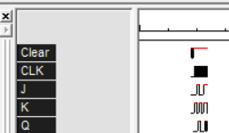
Q is 1 when D is 1 and cp underwent stage of zero to one. If previously, Q was 0 and cp is 1, changing D from 0 to 1 won’t change output until cp is turned zero and one later on.

This is the benefit of edge triggering but also a loss as value is maintained at edges but lost between one half cycle of cp.

**JK Flip Flop IC 74\_73 Test: (74\_76 not found in Logic Works 4.0)**

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**Timing diagram:**



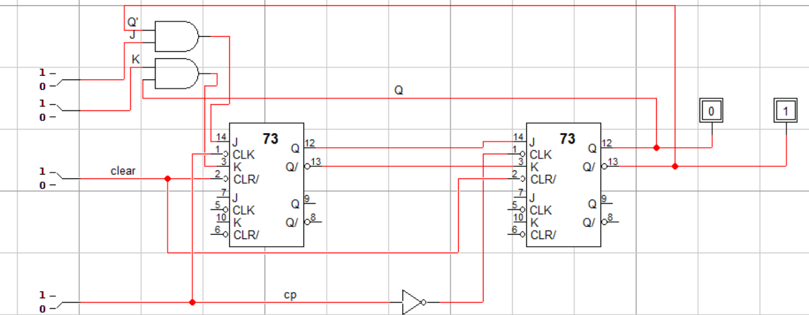
This flip flop has negative edge triggering which updates output (at clear =1) only when CLK is switched off after being ON.

When j and k are 1, output is undefined which is retrieved only when CLK is 0 after staying at 1.

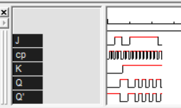
J and K are similar to SR flip flop but SR flip flop has level triggering but JK flip flop has edge triggering (negative at this IC).

**Task 3:**

Perform on Logic Works by using IC of JK-Flip flop and construct master-slave flip flop using JK FF IC.



**Timing diagram:**



When clear is 0, output is 0,1

When clear is 0, output varies by the inputs (j and k). in addition, CP plays a vital role as they perform edge triggering (as displayed by the timing diagram).